POWER TRANSISTOR AMPLIFIER DESIGN USING LARGE-SIGNAL S PARAMETERS*

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Abstract

Large-signal S-parameters are used in the design of UHF power transistor amplifiers, yielding analytical means for calculating stability criteria and circuit impedances for the desired gain and output power. A 3.5 watt, 500 MHz amplifier designed using these methods is described.

Introduction

Small-signal amplifier design methods using the measured small-signal S parameters of the active device are well known.[1-3] The availability of meaningful large-signal transistor S parameters[4] allows these same techniques to be applied to the design of power transistor amplifiers, which until now have required laborious measurements of transistor input and output impedances under the actual desired operating conditions of gain and output power. Such measurements reveal nothing about the circuit's stability if slightly mistuned, nor do they indicate the existence of multiple solutions yielding the same gain, output power, and input VSWR, but with different source and load impedances.

This paper discusses the application of S parameter design methods to power transistor amplifiers, using the measured large-signal transistor parameters. As in the small-signal case, source and load impedances which yield the desired gain and input match are calculated from the S parameters, and stability criteria are given which assure that the resulting circuit will not oscillate. In addition, since output power is not considered in small-signal design, a method is introduced for assuring that the desired output power, as well as gain, is realized.

Design Methods

All of the small-signal amplifier design methods using S parameters[1] can be applied directly to power amplifier design. Briefly, these methods are as follows. The stability factor k, a function of all four S parameters, is first calculated. If $k > 1$, the transistor is unconditionally stable, meaning it will not oscillate with any positive real source or load impedances. In this case the transistor is conjugately matched at input and output, and the gain thus achieved is G_{MAX}.

If $k < 1$, as is the case with most power transistors, the amplifier is only conditionally stable, and will oscillate with some combinations of source and load impedances. It is thus necessary to choose these impedances carefully to prevent oscillation. Further, G_{MAX} is no longer defined, and any desired gain up to infinity (if the circuit is oscillating) can theoretically be achieved. The design method is then to choose the desired gain, and from the S parameters calculate the locus of all load impedances which will yield this gain. This locus is a circle (the constant-gain circle) on the Smith chart. Next, a load impedance on this circle is chosen, and from this and the S parameters the input impedance of the transistor with this load is calculated. The conjugate of this input impedance is chosen for a source so that the input is matched. Finally, input and output instability regions are calculated. These are also circles on the Smith chart, and indicate the source and load impedances which may cause circuit oscillation. In order to assure stability, the chosen source and load should not lie within these instability regions.

In this method, two points are worth noting. First, no attempt is made to match the transistor output impedance, and in fact it is normally mismatched although the input is matched. This situation is familiar to power amplifier designers. Second, in the small-signal case an infinite number of load impedances are possible (all those lying on the constant-gain circle), each yielding a different source impedance. This is obviously not the case in power amplifier design, since the load impedance also affects the power output through the equation $P_{OUT} = (V_{CC} - V_{SAT})^2/2R_{LP}$, where V_{CC} is the collector supply voltage, V_{SAT} is the transistor saturation voltage, and R_{LP} is the parallel equivalent load resistance.** A constant-output-power locus is thus the locus of all load impedances with constant $R_{LP}\left[R_{LP} = \left(R_L^2 + X_L^2\right)/R_L\right.$, where the load impedance $\left.Z_L = R_L + jX_L\right]$. This locus is a constant conductance circle on the Smith chart, passing through the point $Z = R_{LP} + j0$. In general, this constant-power-output circle will intersect the constant-gain circle in two places. These are then the only two impedances which simultaneously yield the desired gain and output power. Each of these two load impedances

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**This expression is strictly correct only for a sinusoidal output voltage waveform, and is normally quite well approximated in a Class-C amplifier operating into a tuned load. Note that the sinusoidal restriction also applies in the measurement of the large-signal S-parameters (see Ref. 4), being accounted for in this case by the use of filters to remove any harmonics present in the untuned circuit.

also produces a different input impedance. Two solutions with different circuit impedances but with the same gain, power output, and input VSWR are thus possible in general. If the desired solution exceeds the power output or gain capability of the transistor, the gain and output power circles will not intersect. At the maximum output power of the transistor these circles will be tangent, giving only one possible solution. Where two solutions are possible, a choice can usually be made on the basis of bandwidth; i.e., one impedance transformation will have a lower Q than the other. This choice can be further aided by a knowledge of the device S-parameters over the frequency band of interest.

Example

A 500 MHz, 3.5 watt amplifier was designed by these methods, using a Power Hybrids PH1003H transistor. This is a common base device rated at 10 dB gain and 3 watts output in the UHF range. The large-signal S parameters of this device were measured and are given in Table 1. From these parameters, a constant 10 dB gain circle and the input and output instability circles were calculated and are shown in Fig. 1. A constant 3.5 watt output power circle, also shown in the figure, was calculated for V_{CC} = 30 volts, assuming V_{SAT} = 0.1 volt. From Fig. 1, it can be seen that the power output and gain circles intersect at Z_{L1} = 46 + j62 and at Z_{L2} = 16 + j42. These two load impedances yield source impedances of Z_{S1} = 4.0 + j1.0 and Z_{S2} = 4.6 + j0.2, both of which are in the stable region defined by the input stability circle.

Each of these two solutions was tested, by adjusting input and output double-stub tuners to the desired source and load impedance and then measuring the resulting amplifier performance. Table 2 gives these measurements. In both cases the gain was 11 dB, compared with the predicted value of 10 dB. The output power was equal to the predicted 3.5 watts in both cases, and the input VSWR was below 1.8:1. The small disparities between measured and predicted performance are felt to be largely due to the presence of harmonics in the input and output voltage waveforms. This excellent agreement between predicted and actual amplifier performance is seen to verify the validity both of the large-signal S parameters and of the design methods in which they are used (at least in this particular case). These methods have also been used successfully in the design of a 35 watt amplifier near 1 GHz using a PH 1025 transistor, which incorporates internal matching by means of MOS capacitors and small lead inductances.

References

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TABLE 1

Large-Signal S Parameters for PHI 1003H at 500 MHz

	S_{11}	S_{12}	S_{21}	S_{22}
Magnitude	.858	.017	.983	1.02
Angle	-178.9	-8.8	-100.2	-78.0

TABLE 2

Measured Amplifier Performance at 500 MHz

	Solution 1	Solution 2
Input VSWR	1.38	1.77
Power Gain	11.0 dB	11.0 dB
Power Output	3.52 W	3.50 W
Z_L	46 + j62	16 + j42
Z_S	4.0 + j1.0	4.6 + j0.2

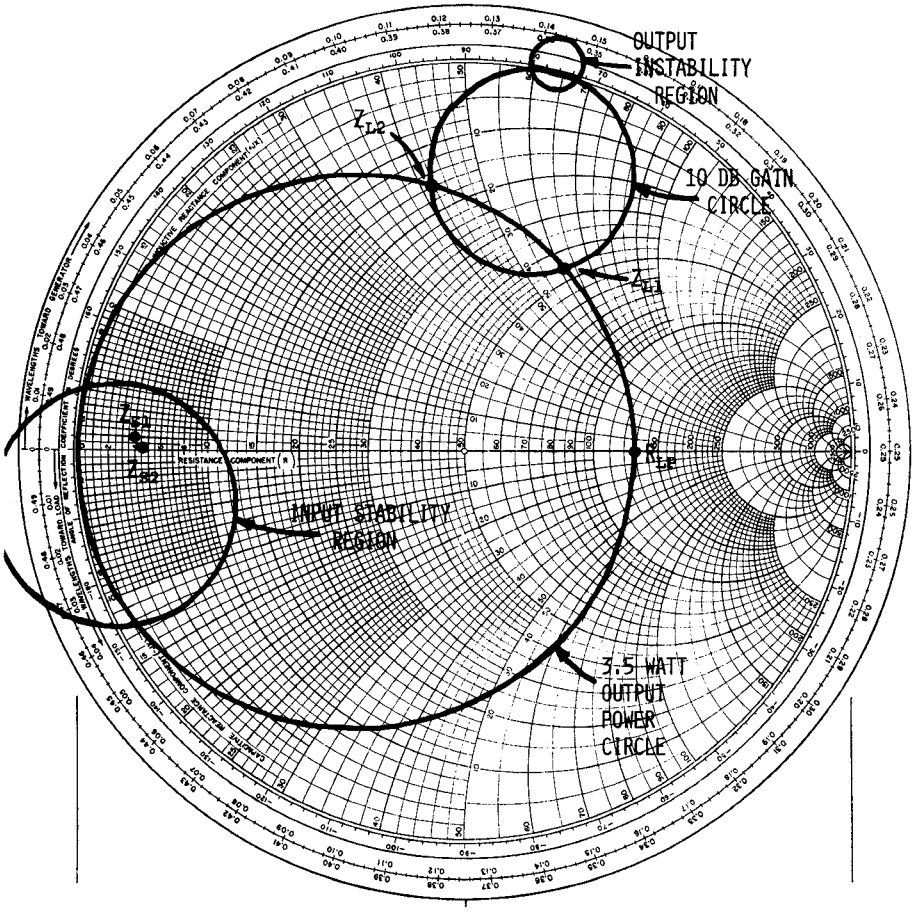

FIGURE 1. 3.5 WATT, 500 MHz AMPLIFIER
DESIGN CALCULATIONS FOR PH1003H.